Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application.

Claim 1 (currently amended): A one-time programming memory element capable of being manufactured in a 0.13μm or below CMOS technology, comprising:

a capacitor having an oxide layer capable of passing direct gate tunneling current;

a write circuit, including

a first switch coupled to said capacitor, said first switch including a first switch transistor connected between a first terminal of said capacitor and a first voltage, and

a second switch coupled to said capacitor, said second switch including a ~~first~~ second switch transistor connected between a second terminal of said capacitor opposing said first terminal and a second voltage; and

a read circuit coupled to said capacitor,

wherein said capacitor is one-time programmable as an anti-fuse by application of a program voltage across said oxide layer via said write circuit to cause direct gate tunneling current to rupture said oxide layer to form a conductive path having resistance of approximately hundreds of ohms or less.

Claim 2 (cancelled)

Claim 3 (previously presented): The one-time programming memory element of claim 1, wherein each of said first and second switch transistors has an oxide layer thicker than said capacitor oxide layer.

Claim 4 (previously presented): The one-time programming memory element of claim 1, wherein said program voltage is equal to a difference between said first and second voltages.

Claim 5 (previously presented): The one-time programming memory element of claim 1, wherein said read circuit comprises plural read switch transistors coupled to said capacitor.

Claim 6 (original): The one-time programming memory element of claim 5, wherein:

when said first and second switch transistors are closed and said read switch transistors are open, one-time programming occurs; and

when said read switch transistors are closed and said first and second switch transistors are open, reading occurs.

Claim 7 (original): The one-time programming memory element of claim 1, wherein said capacitor oxide layer is approximately 20Å thick.

Claim 8 (original): The one-time programming memory element according to claim 1, further comprising a sensing circuit to sense whether said capacitor is programmed.

Claim 9 (original): The one-time programming memory element according to claim 1, wherein a charge pump is not required to program said anti-fuse.

Claim 10 (original): The one-time programming element of claim 1, wherein said program voltage applied across said capacitor oxide layer is less than 7 volts.

Claim 11 (original): The one-time programming memory element of claim 1, wherein when said first and second switches are closed one-time programming occurs.

Claim 12 (original): The one-time programming memory element according to claim 1, wherein said capacitor comprises a field effect transistor having source and drain regions coupled together and to said first switch, a gate coupled to said second switch and a gate dielectric forming said oxide layer.

Claim 13 (original): The one-time programming memory element according to claim 12, wherein said field effect transistor has a deep N-well design including:

a P-well layer adjacent the source and drain regions;

a deep N-well layer below the P-well layer; and

a P-type substrate below the deep N-well layer.

Claim 14 (cancelled)

Claim 15 (previously presented): A process, compatible with 0.13μm or below CMOS technology, for making a one-time programming memory element, comprising the steps of:

forming a capacitor having an oxide layer capable of passing direct gate tunneling current;

forming a write circuit, including the steps of

forming a first switch coupled to the capacitor by connecting a first switch transistor between a first terminal of the capacitor and a first voltage, and

forming a second switch coupled to the capacitor by connecting a second switch transistor between a second terminal of the capacitor opposing the first terminal and a second voltage; and

forming a read circuit coupled to the capacitor,

wherein the capacitor is one-time programmable as an anti-fuse by application of a program voltage across the oxide layer via the write circuit to cause direct gate tunneling current to rupture the oxide layer to form a conductive path having resistance of approximately hundreds of ohms or less.

Claim 16 (cancelled)

Claim 17 (cancelled)

Claim 18 (previously presented): The process of claim 15, wherein each of the first and second switch transistors are formed with an oxide layer thicker than the capacitor oxide layer.

Claim 19 (original): The process of claim 15, wherein said forming a read circuit step comprises the step of forming plural read switch transistors coupled to the capacitor.

Claim 20 (original): The process of claim 15, wherein said forming a capacitor step comprises the step of forming the capacitor oxide layer with a thickness of approximately 20Å.

Claim 21 (original): The process of claim 15, further comprising the step of forming a sensing circuit to sense whether the capacitor is programmed.

Claim 22 (original): The process of claim 15, wherein said forming a capacitor step comprises the step of forming a field effect transistor having source and drain regions coupled together and to the first switch, a gate coupled to the second switch and a gate dielectric forming the oxide layer.

Claim 23 (original): The process of claim 22, wherein said forming a field effect transistor step comprises the steps of:

forming a P-well layer adjacent the source and drain regions;

forming a deep N-well layer below the P-well layer; and

forming a P-type substrate below the deep N-well layer.

Claim 24 (cancelled)